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10/773,283	02/09/2004	Masataka Sasaki	62807-160	3488

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EXAMINER	
KITOV, ZEEV	
ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,283	SASAKI ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on August 15, 2005. Claims 1 – 13 are amended. Applicant's arguments have been given careful consideration but they have been found non-persuasive. The Office Action follows.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 and 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. A reason for that is in the following claim limitation: "logic means for outputting a protection start signal when both the first and second detection signals are being outputted" (emphasis added). In a case when both the collector and the gate voltages exceed their references (V1 and V2) the first and the second comparators issue the logic "0" signals. It is well known property of the comparator that when the signal in its negative input exceeds the signal in its positive input (reference voltage) the comparator issues output logic "0". Therefore, when both the gate and collector voltages

exceed their references both comparators issue logic 0. The logic AND circuit is not intended to detect such event that both inputs are 0, because it cannot distinguish between logic 0 being present in only one of its inputs (when another input signal is logic 1) and presence of zeroes in both inputs. For purpose of examination, the AND gate in the Drawing and Specification and its function were ignored. It was assumed that some unknown logic means performs the disclosed function.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 - 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura et al. (US 5,210,479). Regarding Claim 1, Kimura et al. disclose all the elements of the claim including: a first comparator (elements 12, 13, 15, 23, 3 and 5 in Fig. 8), which detects a collector voltage of the power management semiconductor device and outputs a fist detection signal (base voltage of transistor 15 in Fig. 8) when the detected collector voltage exceeds a first reference voltage (voltage drop across element 14 in Fig. 8); a second comparator (element 31 in Fig. 8) which detects a gate voltage of the power management semiconductor device to output a second detection signal (collector current of transistor 31 in Fig. 8), when the detected gate signal exceeds a second

reference voltage (Vgo), which is a minimum gate voltage for feeding a rated power to said power management semiconductor device or over; logic equivalent means for outputting a protection start signal (collector current of transistor 15 in Fig. 8) when both the first and second detection signals are being outputted; and gate voltage reduction equivalent means (elements 16, 17, 18 and 6 in Fig. 8) reducing the gate voltage in accordance with the protection start signal from the logic means (col. 10, lines 7 – 55).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (US 5,210,479) in view of Topp et al. (US 2004/0075103 A1). Regarding Claim 1, Kimura et al. disclose following elements of the claim including: a first comparator (elements 12, 13, 15, 23, 3 and 5 in Fig. 8), which detects a collector voltage of the power management semiconductor device and outputs a fist detection signal (base voltage of transistor 15 in Fig. 8) when the detected collector voltage

exceeds a first reference voltage (voltage drop across element 14 in Fig. 8); a second comparator (element 31 in Fig. 8) which detects a gate voltage of the power management semiconductor device to output a second detection signal (collector current of transistor 31 in Fig. 8), when the detected gate signal exceeds a second reference voltage (Vgo), which is a minimum gate voltage for feeding a rated power to said power management semiconductor device or over; logic equivalent means for outputting a protection start signal (collector current of transistor 15 in Fig. 8) when both the first and second detection signals are being outputted; and gate voltage reduction equivalent means (elements 16, 17, 18 and 6 in Fig. 8) reducing the gate voltage in accordance with the protection start signal from the logic means (col. 10, lines 7 – 55).

However, it does not disclose the trench type power semiconductor device. Topp et al. discloses the trench IGBT (100 in Fig.7). Both references have the same problem solving area, namely providing the power semiconductor devices, particularly IGBT. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Kimura et al. solution by adding the trench type IGBT according to Topp et al., because as Topp et al. state (col. 2, lines 3 – 10), such device has advantage of lower conducting state voltage drop.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of Topp et al. and Marquardt et al. (US 5,650,906), As was stated above, Kimura et al. and Topp et al. disclose all the elements of Claim 1. However, regarding Claim 2, they do not disclose the voltage divider. Marquardt et al. disclose detection of

the over-voltages by using the resistive voltage divider (58 in Fig. 3, col. 2, lines 58 – 65). It is used for detection of the collector voltage of the IGBT. Both references have the same problem solving area, namely providing over-voltage protection for the IGBT devices. Examiner takes an Official Notice that some operational amplifiers (and comparators as well) allow only a limited voltage between inputs, sometimes as small as +/- 0.5 volt. Particular reference will be provided upon request. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Kimura et al. solution by adding the resistive voltage divider to both the collector and the gate voltage detection according to Marquardt et al., because as Marquardt et al., state (col. 5, lines 27 - 33), "The voltage divider serves the purpose of adjusting the measuring range. The adjustment of the measuring range and a good frequency response can be realized by means of a suitable selection of the resistance values and a required division of the resistor 62 into a plurality of component resistors 66 connected electrically in series". Such adjustment is useful in measuring both the collector and the gate voltage of the IGBT.

Claims 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura in view of Topp et al. and Horowitz et al. textbook, The Art of Electronics. As was stated above, Kimura et al. disclose all the elements of Claims 1 – 4. However, regarding Clams 5 – 8, they do not disclose the first reference voltage as being lower than the line power voltage. Horowitz et al textbook demonstrate that the collector voltage may go beyond the power supply voltage due to inductive load reaction (pages 52 – 53). However, according to them, it may cause breakdown of the switching

transistor. Therefore, the switching transistor is to be protected against voltages exceeding the normal power supply value. Therefore, the first reference voltage used to detect departure of the collector voltage from normal predetermined value in the Kimura et al. circuit must be lower than the line power voltage. Both references have the same problem solving area, namely protecting the power switching transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Kimura et al. solution by setting the first reference voltage lower than the line power voltage, because otherwise the protection circuit of Kimura et al. will become useless.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of Topp et al. Claims 9 and 10 differ from Claims 1 and 2 rejected accordingly by their limitation of both comparators, logic means and gate voltage reduction means and drive circuit being integrated into a single semiconductor integrated circuit. Examiner takes an Official Notice, that today it is common practice in the electronic industry to integrate semiconductor circuits into a common package, i.e. integrated circuit. A particular reference will be provided upon request. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Kimura et al. solution by integrating all the parts of the circuit, except the IGBT, into a single integrated package, because it will reduce the cost, increase the reliability and improve the environmental protection of the circuit.

Claims 11 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wacknov et al. (US 6,812,586) in view of Kimura et al. and Topp et al. Wacknov et al. disclose following elements of the claim: the converter including a power semiconductor device for converting DC current to AC current (element 374 in Fig. 10); a power management semiconductor device (inherent in the structure of the load converter 374 in Fig. 10), which controls a switching operation of said power semiconductor device (elements 514 in Fig. 10). However, it does not disclose the protection circuit for power semiconductor devices. Kimura et al. disclose the protection circuit for power semiconductor devices including: a first comparator (elements 12, 13, 15, 23, 3 and 5 in Fig. 8), which detects a collector voltage of the power management semiconductor device and outputs a fist detection signal (base voltage of transistor 15 in Fig. 8) when the detected collector voltage exceeds a first reference voltage (voltage drop across element 14 in Fig. 8); a second comparator (element 31 in Fig. 8) which detects a gate voltage of the power management semiconductor device to output a second detection signal (collector current of transistor 31 in Fig. 8), when the detected gate signal exceeds a second reference voltage (Vgo), which is a minimum gate voltage for feeding a rated power to said power management semiconductor device or over; logic equivalent means for outputting a protection start signal (collector current of transistor 15 in Fig. 8) when both the first and second detection signals are being outputted; and gate voltage reduction equivalent means (elements 16, 17, 18 and 6 in Fig. 8) reducing the gate voltage in accordance with the protection start signal from the logic means (col. 10, lines 7 – 55). Both references have the same problem solving area, namely driving

the load by power transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Wacknov et al. solution by adding the protection circuit for power semiconductor devices according to Kimura et al. because, as Kimura et al. state (col. 1, lines 31 – 48), the IGBT are especially vulnerable to the short circuit conditions, and therefore should have special protection against that.

Additionally, it does not disclose the trench type power semiconductor device. Topp et al. discloses the trench IGBT (100 in Fig.7). Both references have the same problem solving area, namely providing the power semiconductor devices, particularly IGBT. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Wacknov et al. solution by adding the trench type IGBT according to Topp et al., because as Topp et al. state (col. 2, lines 3 – 10), such device has advantage of lower conducting state voltage drop.

Regarding Claims 12 and 13, Wacknov et al. disclose a hybrid electric vehicle having an internal combustion engine (element 70mn in Fig. 21), an electric motor (element 534 in Fig. 11), a transmission transmitting power from the internal combustion engine and/or the electric motor to wheels, which is inherent in the structure of the hybrid electric vehicle, an inverter unit (element 374 in Fig. 10) converting DC power to AC power, and a DC power storage unit (element 364 in Fig. 6), wherein the electric motor (element 10 in Fig. 2) is an AC motor driven by AC power from the inverter unit (col. 12, lines 30 – 14). As to the inverter unit being the power converter protected against short circuit, Kimura et al. disclose that subject (see Claim 11 rejection above).

Response to Arguments

Applicant argues in his Response about the 35 U.S.C. 112 1st paragraph rejection of Claims 1 and 11. In support of his position Applicant made a reference to the truth table of AND gate. Examiner agrees with the Applicant that AND gate provides logic 1 output when both inputs are supplied with logic 1 signals. However, the problem is that according to Fig. 3 of Drawings, when both the collector and the gate voltages exceed their references (V1 and V2 in Fig. 3) both the first and the second comparators (COMP1 and COMP2 in Fig. 3) issue the logic "0" signals. It is well known property of the comparator that when the signal in its negative input exceeds the signal in its positive input (reference voltage) the comparator issues output logic "0". Therefore, when both the gate and collector voltages exceed their references both comparators issue logic 0. The logic AND circuit is not intended to detect such event that its both inputs are 0, because it cannot distinguish between logic 0 being present in only one of its inputs (when another input signal is logic 1) and presence of zeroes in both inputs. Presence of 0 in one of the inputs of AND gate is sufficient to ensure logic 1 in the output. The rejection is sustained.

The rest of Arguments are based on rejection of Claims 1 and 11 and therefore, are moot in view of given above statement.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
10/30/2005

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